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REMARKS

Claims 1-20, 44, 47, 48, and 50-54 are all the claims pending in the application. Claims 52-54 are added above to further define the invention and claims 45, 46 and 49 are correspondingly canceled. Claims 1-20, 44, 47, 48, 50, and 51 stand rejected on prior art grounds. Applicants respectfully traverse these rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1, 4, 7-10, 44 and 47 stand rejected under 35 U.S.C. §102(b) as being anticipated by Yamanaka (U.S. Patent No. 5,834,797). Claims 2-3 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yamanaka. Claim 5 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Yamanaka in view of Uesugi et al., hereinafter "Uesugi" (U.S. Patent No. 5,708,286). Claims 6, 11-16, 18-20 48, 50, and 51 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yamanaka in view of Pfiester (U.S. Patent No. 5,166,084). Claim 17 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Yamanaka in view of Pfiester and further in view of Uesugi.

Applicants respectfully traverse these rejections based on the following discussion. As explained in greater detail in the specific rebuttal arguments to each of the individual rejections, there are a number of claimed features in the independent and dependent claims that are not taught or suggested in the prior art of record. For example, none of the prior art of record (even the proposed combination of Yamanaka and Pfiester) teaches or suggests a dual gate SOI structure where the upper and lower gates are formed of different materials (independent claim 11). Further, Yamanaka requires that the lower gate be formed from the underlying substrate (which requires that it be silicon based), while the claimed invention provides that the lower gate can be any material (e.g., a metal) and is independent of the underlying insulator layer (dependent claim 52). As another example, with the invention, the thickness and material selection of the

gate dielectrics is independent of the source and drain dielectrics (dependent claims 47 and 51). To the contrary, as clearly shown in Figure 8A of Yamanaka, a single insulator 30 acts as both the gate dielectric and the source/drain dielectric which prevents Yamanaka from disclosing independent gate and source/drain dielectrics. Further, while the Office Action proposes that the structural feature "self-aligned" (independent claims 1, 11, and 44) is a product-by-process limitation, Applicants show below that such actually is a structural feature. With the claimed invention, the upper and lower gate will always be aligned irrespective of manufacturing variations, while the independently patterned upper and lower gates in Yamanaka will demonstrate alignment variations when a number of such structures are compared side-by-side. In addition, there are other patentable features not mentioned here. (For example, dependent claim 54 defines that the channel layer 5 includes an extension 9 into the source and drain regions 11). Thus, as shown below, there are a number of patentable features defined by the claims in the application and the Examiner is respectfully requested to reconsider and withdraw the following rejections.

A. The 102(b)Rejection Based on Yamanaka

Regarding claims 1 and 44, the Office Action states that Yamanaka discloses a transistor comprising (Figs.8A & 8B): a channel region (4); a first gate (G2) on top of said channel region; a second gate (GI) below said channel region; and an isolation layer (3) below said second gate, wherein said first gate and second gate are electrically separated from each other and said first gate and second gate positions said first gate above and aligned with said second gate. The Office Action refers to see Col.12, line 41 - Col.14, line 4. The Office Action recites that although Yamanaka does not explicitly teach the first and second gates are self aligned, "self aligned" is a product-by-process limitation. The Office Action states that the product-by-process claims are given no patentable weight and are directed to the product per se, no matter how actually made.

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—> Applicants respectfully disagree. One ordinarily skilled in this art field understands that the term "self-aligned" defines a structure whereby two features always appear aligned irrespective of manufacturing variations. If one feature is self-aligned with another feature, when multiple devices are compared side-by-side, these two features may move with respect to other structures; however, the two features themselves will always be aligned with respect to one another. This "self-aligned" nature is determined by a manufacturing step, but is still a structural feature.

Independent claims 1 and 44 do not define a processing step and do not qualify as product by process claims. To the contrary, product-by-process claims generally include language similar to "a product formed by a process comprising." Here, there is no processing step defined. The term "self-aligned" includes no processing language but instead defines a structural form of alignment. More specifically items can be a "aligned" which is one formal alignment or "self-aligned" which is a different type of alignment. When items are "aligned" it is intended that they will be aligned, however process manufacturing variations may cause misalignment. To the contrary, the structural term "self-aligned" defines structures that are always aligned with respect to each other irrespective of any type of misalignment that may occur during manufacturing.

Yamanaka describes an upper and lower gate that are merely "aligned" while the claimed invention describes a fundamentally different structure whereby the upper and lower gates will always be aligned, irrespective of processing misalignments (self-aligned). Therefore, Applicants submit that the claimed term "self-aligned" in independent claims 1 and 46 is a structural feature which is understood by those ordinarily skilled in the art to mean that these two features (first gate and second gate) will always be aligned with each other, irrespective of manufacturing variations and irrespective of their alignment with respect to other features of the structure.

This structural self-aligned feature is clearly not taught or suggested by Yamanaka because the lower gate G1 is formed using a first mask shown in Figure 7B of Yamanaka while the second gate G2 is formed using a different mask in a different processing step, as shown in

Figure 8A of Yamanaka (also see column 13, lines 41-43). In Yamanaka the two gates G1, G2 are formed using different masks and differ processing steps. As is well known to those ordinarily skilled in the art, these different masks will sometimes be misaligned which will cause the upper and lower gates to be misaligned. Therefore, the structure disclosed by Yamanaka as understood by one ordinarily skilled in the art is different than the "self-aligned" structure defined by independent claims 1 and 44 and Yamanaka does not teach or suggest the structure defined by independent claims 1 and 44.

→ Regarding claim 47, the Office Action states that Yamanaka discloses (Figs. 8A & 8B): source and drain regions laterally adjacent said channel region, said first gate, and said second gate; and source and drain dielectric between said source and drain regions and said first gate and said second gate, wherein a thickness and material selection of said first gate dielectric and said second gate dielectric is independent of said source and drain dielectrics.

With the claimed invention, the thickness and material selection of the gate dielectrics is independent of the source and drain dielectrics (dependent claim 47). As shown in Applicants' Figure 11, the source/drain dielectric 10 is formed during a different processing step than when the gate oxides 1, 6 are formed as shown in Figures 1, 5, and 6. Therefore, with the inventive structure, the material selection and thickness of the gate dielectrics is independent of that of the source and drain dielectrics. This is important for a number of reasons including that it is often desirable to have a very thin gate dielectric to provide for very fast switching and low-power operation of the channel region. To the contrary, it is desirable to have thicker source/drain dielectrics to prevent excessive capacitance. To the contrary, as clearly shown in Figure 8A of Yamanaka, a single insulator 30 acts as both the gate dielectric and the source/drain dielectric which prevents Yamanaka from disclosing independent gate and source/drain dielectrics. Therefore, with the structure disclosed in Yamanaka, there can be no difference between the material and thickness of the gate dielectrics and the source/drain dielectrics and Yamanaka does not teach or suggest the invention defined by dependent claim 47.

Thus, as shown above, independent claims 1 and 44 are patentable over Yamanaka. Further, dependent claims 4, 7-10, and 47 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define (e.g., see the example of dependent claim 47 discussed above). In view the forgoing, the Examiner is respectfully requested to reconsider and withdraw this rejection

B. The 103(a) Rejection Based on Yamanaka

The Office Action states that claims 2-3 are rejected because Yamanaka teaches substantially the entire claimed structure, applied to claim 1 as explained above, except that the first gate comprises a different doping concentration and doping species than said second gate. The Office Action argues that it is, however, well known in the art to select the concentration of gate electrode to adjust a threshold voltage in the transistor. The Office Action recites that if the first gate electrode has a lower concentration than the second gate electrode, a threshold voltage of the first gate is lower than that of the second gate. The Office Action concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have formed Yamanaka's "first and second gate" having a different concentration, since the different concentration of gate electrode provides the different threshold voltage in device.

In response, Applicants respectfully submit that the teachings in Yamanaka are very clear and require that the first gate electrode G1 and the second gate electrode G2 each comprise a polycrystalline silicon film (column 11, lines 12-13). Thus, Yamanaka clearly teaches that the gates are identical and there is no teaching or suggestion that they should be otherwise. The proposal made in the Office Action for modifying Yamanaka is not supported by any teaching other than the supposition that some benefit may accrue. 35 U.S.C. §103 requires that there be some objective teaching for the modification of a reference. Here there is none.

Further, as shown above, independent claim 1 is patentable over Yamanaka. Therefore, dependent claims 2-3 are similarly patentable, not only by virtue of their dependency from a

patentable independent claim, but also by virtue of the additional features of the invention they define. In view the forgoing, the Examiner is respectfully requested to reconsider and withdraw this rejection

C. The Rejection Based on Yamanaka in view of Uesugi

Regarding claim 5, the Office Action states that Yamanaka fails to teach the conductive contact of the first gate and second conductive contact of the second gate are coplanar, but that Uesugi teaches in Fig. 1 and Col. 7, lines 42-46, the first conductive contact (80) of the first gate (60) and the second conductive contact (90) of the second gate (30) are coplanar. The Office Action concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Uesugi with Yamanaka's device in order to reduce the manufacturing processing.

Uesugi discloses a vertical semiconductor device having an insulated gate structure that makes use of a double-gate structure. The double-gate structure dramatically reduces the channel resistance, JFET resistance, and epitaxial resistance of the on-resistance of the power MOSFET, and implements an adequate breakdown voltage due to the effect of gate bias. In principle, a first gate and second gate having mutually facing portions are driven synchronously. This causes first and second channels to be formed in correspondence with first and second gates, and the currents flowing through these first and second channels form the on-current for this power device having a vertical structure.

As shown above, Yamanaka does not teach or suggest the invention as defined by independent claim 1 because Yamanaka fails to teach a number of features defined by independent claim 1, including the upper and lower gates being "self-aligned." Uesugi is referenced for the limited purpose of allegedly showing coplanar contacts. However, Uesugi does not teach or suggest upper and lower gates that are aligned (much less self-aligned). To the contrary, the upper gate 60 and lower gate 30 shown in Figure 41 of Uesugi actually affect

different channel regions (ch1, ch2) and are not truly upper and lower gates that border a channel region. Further, as illustrated by Figure 41 of Uesugi, the gates 30, 60 are not aligned.

Therefore, Applicants respectfully submit that if one ordinarily skilled in the art had combined Yamanaka and Uesugi as suggested in the Office Action, any such combination would not teach or suggest a structure having "self-aligned" upper and lower gates, as defined by independent claim 1. Therefore, independent claim 1 is patentable over the combination of Yamanaka and Uesugi suggested in the Office Action. Further, dependent claim 5 is similarly patentable, not only by virtue of its dependency from a patentable independent claim, but also by virtue of the additional features of the invention it defines. In view the forgoing, the Examiner is respectfully requested to reconsider and withdraw this rejection

D. The Rejection Based on Yamanaka in view of Pfiester

Regarding claim 11, the Office Action states that Yamanaka discloses a semiconductor chip having at least one transistor, said transistor comprising (Figs. 8a & 8B): a channel region (4); a first gate (02) on top of said channel region; a second gate (01) below said channel region; and an isolation layer (3) below said second gate. See also Col.12, line 41 -Col.14, line 4. The Office Action declares that although Yamanaka does not explicitly teach that the first and second gates are self-aligned, but that "self-aligned" is a product-by-process limitation. The Office Action renders that the product-by-process claims are given no patentable weight.

The Office Action further states that although Yamanaka does not explicitly teach that the first gate comprises a different material than said second gate, the Office Action argues that Pfiester teaches in Fig.4 that the first gate electrode (24) comprises a different material than said second gate electrode (26). The Office Action determines that it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of

Pfiester into Yamanaka's device, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Pfiester discloses a process for fabricating an isolated silicon on insulator (SOI) field effect transistor (FET) (10, 11, 13, 15). The SOI FET is made on a substrate material (12). In one form, a first control electrode referred to as gate (24), is contained within the substrate (12) underlying a dielectric layer (14). A second control electrode referred to as gate (26) overlies a dielectric layer (28). A source and a drain current electrode are formed from a germanium-silicon layer (18). A silicon layer (16) forms an isolated channel region of the SOI FET. The gates (12, 24) are separated from the channel by gate dielectric layers (14, 28). The germanium-silicon layer (18) is much thicker than the silicon layer (16) which is made thin to provide a thin channel region. An optional nitride layer 20 overlies the germanium-silicon layer (18).

As shown above, Yamanaka does not teach or suggest the invention as defined by independent claim 11 because Yamanaka fails to teach a number of features defined by independent claim 11, including the upper and lower gates being "self-aligned." The Office Action makes reference to Pfiester for allegedly teaching that the first gate electrodes can comprise a different material than the second gate electrodes. However, Pfiester actually forms the lower gate 24 by doping a portion of the substrate 12. Therefore, Pfiester cannot teach or suggest upper and lower gates that are "self-aligned" with each other. The actual alignment of the lower gate 24 is imprecise because this gate is formed in an implantation process. The amount by which the impurity spreads within the substrate 12 within Pfiester is highly uncontrolled. Therefore, the size of the gate will not be truly "self-aligned" within the meaning of the claimed invention, because the claimed structure produces a tightly controlled size of each of the gates.

Further, Pfiester does not teach or suggest that the first gate "comprises a different material than said second gate" as defined by independent claim 11. To the contrary, the lower gate 24 in Pfiester is merely a doped region of the substrate and is not truly a separate gate

material. Thus, the doped region 24 within Pfiester would not teach or suggest to one ordinarily skilled in the art the second gate that is defined by independent claim 11. The doping concentrations that are used to change the conductivity of a silicon substrate are extremely small on the molecular level (only a few percent) and do not actually create a separate material. Therefore, Pfiester does not actually teach a separate lower gate, but instead merely teaches a region within the substrate which is has slightly different chemical properties from the surrounding substrate. Thus, there will not be any structural "self-aligned" upper and lower gates as defined by independent claim 11, if one ordinarily skilled in the art were to make a structure according to the teaching within Pfiester and/or Yamanaka. Therefore, Applicants submit that even if one ordinarily skilled in the art had combined Yamanaka and Pfiester, as proposed in the Office Action, the combination would not teach or suggest the invention as defined by independent claim 11.

Regarding claim 51, the Office Action argues that Yamanaka as modified by Pfiester discloses (Figs. 8A & 8B): source and drain regions laterally adjacent said channel region, said first gate, and said second gate; and source and drain dielectric between said source and drain regions and said first gate and said second gate, wherein a thickness and material selection of said first gate dielectric and said second gate dielectric is independent of said source and drain dielectrics.

With the claimed invention, the thickness and material selection of the gate dielectrics is independent of the source and drain dielectrics (dependent claim 51). As shown in Applicants' Figure 11, the source/drain dielectric 10 is formed during a different processing step than when the gate oxides 1, 6 are formed as shown in Figures 1, 5, and 6. Therefore, with the inventive structure, the material selection of the gate dielectrics is independent of that of the source and drain dielectrics. This is important for a number of reasons including that it is often desirable to have a very thin gate dielectric to provide for very fast switching and low-power operation of the channel region. To the contrary, it is desirable to have thicker source/drain dielectrics to prevent excessive capacitance. To the contrary, as clearly shown in Figure 8A of Yamanaka, a single

insulator 30 acts as both the gate dielectric and the source/drain dielectric which prevents Yamanaka from disclosing independent gate and source/drain dielectrics. Therefore, with the structure disclosed in Yamanaka, there can be no difference between the material and thickness of the gate dielectrics and the source/drain dielectrics and Yamanaka does not teach or suggest the invention defined by dependent claim 51.

Therefore, Applicants submit that even if one ordinarily skilled in the art had combined Yamanaka and Pfiester, as proposed in the Office Action, the combination would not teach or suggest the invention as defined by independent claim 11. Thus, independent claim 11 is patentable over the proposed combination. Further, dependent claims 6, 14, 16, 18-20, and 48-51 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define (see the example of dependent claim 51 discussed above). In view of the forgoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

E. The Rejection Based on Yamanaka in View of Pfiester and Further in View of Uesugi

With respect to claim 17, the Office Action declares that Yamanaka as modified by Pfiester applies to claim 11 above. The Office Action argues that although Yamanaka as modified by Pfiester fails to teach that the first conductive contact of the first gate and the second conductive contact of the second gate are coplanar, that Uesugi teaches that in Fig.1 & Col.7, lines 42-46 the first conductive contact (80) of the first gate (60) and the second conductive contact (90) of the second gate (30) are coplanar. Therefore, the Office Action concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of Uesugi with Yamanaka's device in order to reduce the manufacturing processing.

However, as explained above Uesugi does not teach or suggest upper and lower gates that are aligned (much less self-aligned). To the contrary, the upper gate 60 and lower gate 30 shown in Figure 41 of Uesugi actually affect different channel regions (ch1, ch2) and are not truly upper and lower gates that border a channel region. Further, as illustrated by Figure 41 of Uesugi, the gates 30, 60 are not aligned.

Therefore, Applicants respectfully submit that if one ordinarily skilled in the art had combined Yamanaka, Pfiester, and Uesugi as suggested in the Office Action, any such combination would not teach or suggest a structure having "self-aligned" upper and lower gates, as defined by independent claim 11. Therefore, independent claim 11 is patentable over the combination of Yamanaka, Pfiester and Uesugi suggested in the Office Action. Further, dependent claim 17 is similarly patentable, not only by virtue of its dependency from a patentable independent claim, but also by virtue of the additional features of the invention it defines. In view the forgoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

II. Formal Matters and Conclusion

As shown above, there are a number of claimed features in the independent and dependent claims that are not taught or suggested in the prior art of record. For example, none of the prior art of record (even the proposed combination of Yamanaka and Pfiester) teaches or suggests a dual gate SOI structure where the upper and lower gates are formed of different materials (e.g., independent claim 11). Further, Yamanaka requires that the lower gate be formed from the underlying substrate (which requires that it be silicon based), while the claimed invention provides that the lower gate can be any material (e.g., a metal) and is independent of the underlying insulator layer (dependent claim 52). As another example, with the invention, the thickness and material selection of the gate dielectrics is independent of the source and drain dielectrics (dependent claims 47 and 51). To the contrary, as clearly shown in Figure 8A of

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Yamanaka, a single insulator 30 acts as both the gate dielectric and the source/drain dielectric which prevents Yamanaka from disclosing independent gate and source/drain dielectrics. Further, while the Office Action proposes that the structural feature "self-aligned" (independent claims 1, 11, and 44) is a product-by-process limitation, Applicants have shown above that such actually is a structural feature. With the claimed invention, the upper and lower gate will always be aligned irrespective of manufacturing variations, while the independently patterned upper and lower gates in Yamanaka will demonstrate alignment variations when a number of such structures are compared side-by-side. In addition, there are other patentable features not mentioned here (for example, dependent claim 54 defines that the channel layer 5 includes an extension 9 into the source and drain regions 11). Thus, as shown above, there are a number of patentable features defined by the claims in the application and the Examiner is respectfully requested to reconsider and withdraw the following rejections.

In view of the foregoing, Applicants submit that claims 1-20, 44, 47, 48, and 50-54, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 50-0510.

Respectfully submitted,

Dated: 11/19/02

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Marked Up Version of Changes Made:

Please cancel claims 45, 46 and 49.

Please add the following new claims.

52. The transistor in claim 1, wherein a material composition of said second gate is independent of a material composition of said isolation layer.

53. The transistor in claim 1, wherein said channel region comprises single crystal silicon.

54. The transistor in claim 44, wherein said channel region includes an extension into said source and drain regions.